45533

MEMORY CONTROL APPARATUS AND METHOD FOR DIGITAL SIGNAL PROCESSING

[0001] This application claims priority from the Korean Patent Application No. 2002-0074893, filed on November 28, 2002, which is incorporated in full herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention:

[0002] The present invention relates to a memory control apparatus and method for digital signal processing, and more particularly, to a system and method for operating a plurality of digital signal processors using one memory card.

Description of the Related Art:

[0003] Generally, a digital signal processor (hereinafter referred to as "DSP") is used for real-time processing of a digital signal. The digital signal typically includes data representing a serial number or a digital value used for indicating the corresponding analog signal. The DSP is used in diverse fields including an audio system such as a small-sized disc player, a radio communication system such as a cellular phone, a digital still camera (hereinafter referred to as "DSC"), and a digital video camera (hereinafter referred to as "DVC").

[0004] Recently, with the demand for combined appliances, the development of a dual appliance having two or more functions has increased remarkably. In particular, techniques for implementing a DVD for taking a moving image and a DSC for recording a still image into one appliance have been used significantly.

[0005] A technique of integrating the DSC and the DVC in the related art is illustrated in FIGs. 1 and 2. FIG. 1 is a perspective view of an apparatus for taking an image, in which a digital still camera and a digital video camera are integrated according to the related art, and FIG. 2 is a block diagram of the apparatus illustrated

in FIG. 1. Referring to FIGs. 1 and 2, the body 10 of the apparatus includes a DSC signal conversion unit 40, a DVC signal conversion unit 45, a still image codec unit 50, a moving image codec unit 55, a storage unit 60, an input unit 70, a display unit 80, and a control unit 90.

[0006] A camera part 20 includes a housing 15 rotatably installed on the body 10 within a predetermined angle, a first camera 22 for taking a still image, and a second camera 24 for taking a moving image. The first camera 22 and the second camera 24 are arranged to face each other.

[0007] Accordingly, the camera part 20 rotates clockwise or counterclockwise at a predetermined angle on an rotating axis X, and it is preferable that the camera part 20 rotates to the extent that a DSC lens group 22a and a DVC lens group 24a maintain balance with an image-taking direction A. That is, as shown in FIG. 2, it is preferable that, if the housing 15 is manually rotated at an angle of 180° or about 180°, the positions of the DSC lens group 22a and the DVC lens group 24a change the directions in which they are facing.

[0008] The first camera 22 has a DSC lens group 22a, a DSC driving unit 22b, a DSC detection unit 22c, and a DSC image pickup unit 22d. The DSC lens group 22a is for taking a still image, and the DSC driving unit 22b moves a DSC zoom lens (not illustrated) and a DSC focus lens (not illustrated) under the control of the control unit 90. The DSC detection unit 22c is a sensor for detecting the position of a lens under the control of the control unit 90, and the DSC image pickup unit 22d converts the image signal of an object, which has passed through the DSC zoom lens (not illustrated) and the DSC focus lens (not illustrated), into an electric image signal using a charge coupled device or any other suitable component.

[0009] The second camera 24 also has a DVC lens group 24a, a DVC driving unit 24b, a DVC detection unit 24c, and a DVC image pickup unit 24d, and its operation is the same as that of the first camera.

[0010] The DSC signal conversion unit 40 and the DVC signal conversion unit 45 remove noise included in electric signals output from the DSC image pickup unit 22d and the DVC image pickup unit 24c, and amplify gains so that the converted electric

image signals are output with a constant or a substantially constant level. Also, the DSC signal conversion unit 40 and the DVC signal conversion unit 45 convert the electric analog signals into digital image signals, and output automatic control data through digital processing.

[0011] The still image codec unit 50, under the control of the control unit 90, compresses the still image signal output from the DSC signal conversion unit 40 using a compression system such as JPEG. The compressed still image data is stored in a storage medium such as a flash memory 62 of the storage unit 60.

[0012] The moving image codec unit 55, under the control of the control unit 90, compresses the moving image signal output from the DVC signal conversion unit 45 using a compression system such as JPEG. The compressed moving image data is stored in a storage medium such as a tape 64 of the storage unit 60.

[0013] If a reproduction command signal for reproducing the stored image signal is input through the input unit 70, the still image codec unit 50 and the moving image codec unit 55 discontinue the compression of the coded data stored in the flash memory 62 and the tape 64, respectively, under the control of the control unit 90.

[0014] For example, if a reproduction command signal for reproducing the still image signal is input through the input unit 70, the still image codec unit 50 discontinues the compression of the coded still image data stored in the flash memory 62, and outputs the still image data to the display unit 80.

[0015] The input unit 70 has an image-taking key 70a for providing an image-taking command signal to the control unit 90, and a plurality of manipulation buttons (not illustrated) for performing a plurality of functions. The display unit 80 has a viewfinder 82 or an LCD panel 84 provided in one side of the main body 10. The display unit 80 displays the image taken through the DSC 22 or DVC 24 or the compression-released image under the control of the control unit 90.

[0016] The control unit 90 controls the entire operation of the image-taking apparatus using various kinds of control programs stored in the storage unit 60 and the automatic control data outputted from the DSC signal conversion unit 40 or the DVC signal conversion unit 45. The control unit 90 determines what the selected image-

taking mode is by an output signal of a mode sensing unit 30, and drives the camera part 20 corresponding to the selected image-taking mode. For example, if signals which indicate an on state of the DSC 22 and an off state of the DVC 24 are input from the mode sensing unit 30, the control unit 90 determines that the image-taking mode of the camera part 20 is the still image mode. Also, if the image-taking command signal is applied from the image-taking key 70a, the control unit 90 drives the DSC 22 corresponding to the still image mode. If a record command signal is applied from the input unit 70, the control unit 90 controls the still image codec unit 50 to compress the image signal of the object, while if a reproduction command signal is applied, it controls the still image codec unit 50 to discontinue the compression of the image signal, and then displays the image signal on the display unit 80.

[0017] As described above, the DSC and the DVC have memories for storing image information, respectively, and in the case of integrating the two appliances, the size of the digital camera is increased, and the operating system for controlling the respective systems becomes complicated.

SUMMARY OF THE INVENTION

[0018] Therefore, an object of the present invention is to provide a memory control apparatus and method for digital signal processing, and more particularly, a system and method for operating a plurality of digital signal processors using one memory card.

[0019] Accordingly, an embodiment of the present invention provides a memory control apparatus and method, adapted to operate with a plurality of digital signal processors (DSPs). The memory control apparatus and method employ a switch, adapted to selectively route signals for input to the DSPs from a memory and for output from the DSPs to the memory, a buffer, adapted to selectively output to the DSPs memory information indicating that the memory is available, and a controller, adapted to control the switch to route the signals to and from the memory and DSPs and to control the buffer to selectively output the memory information. The memory

is a removable memory, such as a flash memory, and the memory information indicates that the memory has been inserted into a port for access by the memory control apparatus. The switch includes a plurality of selection switches, coupled between the DSPs and the memory, which are controlled by the controller. The buffer includes a three-state buffer which selectively outputs the memory information of the memory to the DSPs as controlled by the controller.

[0020] The apparatus and method further employ a key input unit, adapted to indicate an operation mode, such that the control unit controls recording of data in the memory or reproduction of data from the memory according to the operation mode indicated by the key input unit. It is also noted that one of the DSPs is employed with a digital still camera and another of the DSPs is employed with a digital video camera, and the controller controls the switch to route the signals to and from the memory and the DSPs of the digital still camera and digital video camera.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The above objects and other advantages of the present invention will become more apparent by describing in detail the preferred embodiments thereof with reference to the attached drawings in which:

[0022] FIG. 1 is a perspective view illustrating an apparatus for taking an image, in which a digital still camera and a digital video camera are integrated according to the related art;

[0023] FIG. 2 is a block diagram of the apparatus illustrated in FIG. 1;

[0024] FIG. 3 is a block diagram illustrating main signal processing blocks according to an embodiment of the present invention; and

[0025] FIG. 4 is a flowchart illustrating a main signal process according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0026] A memory control apparatus and method for a digital signal process according to a preferred embodiment of the present invention will now be described in detail with reference to the annexed drawings in which like reference numerals refer to like elements.

[0027] FIG. 3 is a block diagram illustrating main signal processing blocks according to an embodiment of the present invention. The numerals of the general constituent elements for the digital process, which are identical or substantially identical to those of the related art of FIG. 2, and the explanation of such constituent elements will thus be omitted. In FIG. 3, the memory control apparatus for a digital signal process includes a signal processing unit 100 for a digital still camera (hereinafter referred to as "DSP-1"), a signal processing unit 200 for a digital video camera (hereinafter referred to as "DSP-2"), a memory stick 500, a selection switch 300, a three-state buffer 400, a key input unit 700, and a control unit 600.

[0028] The DSP-1 100 and the DSP-2 200 process digital signals of the digital still camera and the digital video camera, respectively. The DSP-1 and the DSP-2 have interface units 110 and 210 for performing a digital signal input/output with the memory stick 500, and the interface units 110 and 210 are respectively provided with clock terminals (SCLK) 120 and 220, data terminals (SDIO) 160 and 260, enable terminals (BS) 140 and 240, and insert-1 and insert-2 terminals 170 and 270 which are signal terminals which indicate that the memory stick 500 has been inserted.

[0029] The memory stick 500 can record or reproduce the digital signal, and has a clock terminal (SCLK), a memory stick enable terminal (BS), a data terminal (SDIO), and an insert terminal for outputting a signal for indicating that the memory stick 500 has been inserted.

[0030] Also, the memory stick 500 may be a semiconductor type flash memory which can be installed in the signal processing apparatus, or a card type flash memory such as C.F CARD, SD CARD, SMC CARD, MMC CARD, and so on, which is detachable from the apparatus. The selection switch 300 selects and connects signals input/output among the DSP-1 100, the DSP-2 200 and the memory stick 500.

[0031] The three-state buffer 400 receives the insert signal which indicates the insertion of the memory stick 500, and outputs the insert signal to the insert-1 and insert-2 terminals 170 and 270 under the control of the control unit 600, so that the respective DSPs can communicate with the memory stick 500. The control unit 600 receives the key input from the key input unit 700, and outputs a control signal 620 for switching the selection switch 300 and a control signal 630 for controlling the three-state buffer 400. The control unit 600 also controls the entire system.

[0032] The key input unit 600 is provided with a key for selecting a DSC mode and a DVC mode, and system control keys for the recording/reproducing operation. Preferably, the mode selection may be performed through a rotary contact switch operable without a separate key input. That is, the rotary contact switch senses the image-taking mode corresponding to the digital still camera or the digital video camera in accordance with the rotating angle of the camera part 20 with respect to the main body 10 as shown in FIG. 1. More preferably, it senses the image-taking mode corresponding to the camera part 20 based on an angle of 180° or about 180° when the camera part 20 is rotated.

[0033] An example of the operation of the memory control apparatus for a digital signal process as described above will now be explained.

[0034] FIG. 4 is a flowchart illustrating an example of the operation of the memory control apparatus for a digital signal process according to an embodiment of the present invention.

[0035] The control unit 600 determines whether the present mode is a read mode or a write mode through the key input unit 700 (step S10), and if it is determined that the present mode is the read mode, it determines whether the memory stick 500 is inserted by interpreting the insert signal (step S11). At this time, if it is determined that the memory stick 500 is not inserted, the control unit 600 controls an OSD (On-Screen Display) unit (not illustrated) to display that the memory stick 500 is not inserted (step S12). Then, the control unit 600 determines whether to select the DSP-1 mode or the DSP-2 mode through the key input unit 700 (step S13). If the DSP-1 mode, that is, the digital still camera mode, is selected (step S14), the control unit 600

controls the selection switch 300, so that the signals of the memory stick 500 can be connected to the respective terminals of the DSP-1. Specifically, it controls the clock terminal SCLK of the memory stick 500 to be connected to the clock terminal (SCLK) 120 of the DSP-1 100, and controls outputs of the enable terminal BS and the data terminal SDIO of the memory stick to be connected to the enable terminal (BS) 140 and the data terminal SDIO of the DSP-1 100, respectively. The control unit 600 simultaneously outputs the control signal 630 for providing to the DSP-1 100 the insert signal which indicates the insertion of the memory stick 50, and which is input to the three-state buffer 400.

[0036] Also, the control unit 600 controls the system so that the DSP-1 100 reproduces the digital signal stored in the memory stick 500 and displays the reproduced signal on the display unit (not illustrated).

[0037] If the DSP-2 mode, that is, the digital video camera mode, is selected at step S13 (step S15), the control unit 600 controls the selection switch 300 through the same process as above, so that the respective terminal signals of the memory stick 500 are connected to the respective terminals of the DSP-2. The control unit 600 simultaneously outputs the control signal 630 for providing to the DSP-2the insert signal which indicates the insertion of the memory stick 500, and which is input to the three-state buffer 400. Also, the control unit 600 controls the system so that the DSP-2 200 reproduces the digital signal stored in the memory stick 500 and displays the reproduced signal on the display unit (not illustrated).

[0038] Alternatively, if the write mode is selected at step S10, the control unit 600 determines whether the memory stick 500 is inserted by interpreting the insert signal (step S21). At this time, if it is determined that the memory stick 500 is not inserted, the control unit 600 controls the OSD unit (not illustrated) to display that the memory stick 500 is not inserted (step S22). Then, the control unit 600 determines whether to select the DSP-1 mode or the DSP-2 mode through the key input unit 700 (step S23). If the DSP-1 mode, that is, the digital still camera mode, is selected (step S24), the control unit 600 controls the selection switch 300, so that the signals of the respective terminals of the DSP-1 can be connected to the terminals of the memory stick 500.

[0039] The control unit 600 simultaneously outputs the control signal 630 to provide to the DSP-1 the insert signal indicating the insertion of the memory stick 500, which is input to the three-state buffer 400. Also, the control unit 600 controls the system so that the signals output from the DSP-1 200 are stored in the memory stick 500.

[0040] If the DSP-2 mode, that is, the digital video camera mode, is selected at step S23 (step S25), the control unit 600 controls the selection switch 300 through the same process as above, so that the output signals of the respective terminals of the DSP-2 are connected to the respective terminals of the memory stick 500. The control unit 600 simultaneously outputs the control signal 630 for providing the insert signal, which is input to the three-state buffer 400, to the DSP-2 200. Also, the control unit 600 controls the system so that the output signals of the DSP-2 200 are stored in the memory stick 500.

[0041] According to the memory control apparatus and method for digital signal processing of the embodiment of the present invention described above, the memory and the buffer are commonly used when a plurality of DSPs are processed, and thus an operation system having a simple construction is provided.

[0042] While an embodiment of the present invention has been described in detail, it should be understood that various changes, substitutions and alterations can be made hereto without departing from the spirit and scope of the invention as defined by the appended claims.